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CHARGE ANALYSIS PREDICTIONS AND MEASUREMENTS OF STORAGE TIME FOR A SWITCHING TRANSISTOR

by

Bruce Gene DeLugish

September 1, 1968



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Report No. 279

CHARGE ANALYSIS PREDICTIONS AND MEASUREMENTS OF STORAGE TIME FOR A SWITCHING TRANSISTOR *

bу

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September 1, 1968

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1. INTRODUCTION

Most of the transistor circuits employed in digital systems operate the transistors in a nonlinear manner as the basis for establishing two distinct ranges of output variables. Circuits discriminate more accurately between the ranges of values of the input variable, and produce outputs which are less sensitive to transistor parameters and other components, and are thus better quantized, if the circuit operates in a distinctly nonlinear manner. Use of such extreme nonlinearity amounts to using ON and OFF states.

Digital circuits can be classified on the basis of the transistor operating conditions which correspond to the two states of the circuit. Such circuits can be divided into two classes: saturating and nonsaturating. In saturating switching circuits, one state corresponds to the saturation region of operation where both junctions are forward biased, and the other state corresponds to operation in the cut-off region where both junctions are reverse biased, or possibly the active region where the emitter is forward biased and the collector is reverse biased. In nonsaturating switching circuits, one state corresponds to operation in the active region and the other state normally to operation in the cut-off region. It is also possible that both states correspond to operation in the active region. In any case, the two states must correspond to distinctly different operating points.

Although saturating switching ciruitry is inherently slower than nonsaturating circuitry (see below), it is still widely used today.

Saturating circuits are easier to design and are more reliable because

they are less susceptible to variations of transistor parameters and other components. The saturated transistor also offers the advantage that it presents very low input and output impedances. Because of this low impedance and the lesser susceptibility to variation of parameters, saturating circuits are also easier to interface.

Saturating circuitry is inherently slower than nonsaturating circuitry because of the phenomenon of storage time. When switching a transistor from the ON state (saturated region of operation) to the OFF state (cut-off or active region of operation), it is observed that the collector current waveform does not immediately follow the base current waveform. (It is assumed that the base current, externally controlled, is a square pulse.) Instead the collector current is observed to stay relatively constant at its saturation value for a certain period of time and then finally decrease (approximately exponentially) to its new equilibrium value in the active or cut-off region. The time delay before the collector current begins to fall is the storage time delay.

A knowledge of the storage time delay is essential in the design of saturating transistor switching circuits. An accurate prediction formula in terms of known or easily measured parameters would certainly be of value to the circuit designer. Several prediction equations have been produced; the best known are those of Ebers and Moll² and Beaufoy and Sparkes.³ The advantage of the charge analysis approach of Beaufoy and Sparkes is that the prediction formula achieved depends on only two transistor parameters, whereas the formula of Ebers and Moll depends on four parameters. A derivation of the charge analysis prediction equation, along with some discussion of its limiting assumptions, is presented in the next section.

The purpose of this paper is to test the accuracy and validity of this prediction equation for a switching transistor. To this end, storage time measurements for a variety of current conditions were taken. A sample of sixty units was tested in order to achieve a reasonable confidence level in the validity of the results. Measuring such a sample, as opposed to measuring a single transistor, puts some restrictions on the measurement technique and the number of different measurements that can be taken in a limited amount of time. These limitations are discussed further in a later section.

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2. THE PHENOMENON OF STORAGE TIME

Let us consider the transistor circuit shown in Figure 1. Suppose that we increase the value of I_B from zero to some small positive value. As we do so, the collector current I_C increases with it, since we are in the active region of the transistor where the collector current is proportional to the base current. In the active region the emitter is forward biased and the collector is reverse biased, but as we increase the base current further a condition is eventually reached by virtue of the increased voltage across the load resistor so as to make the voltage between the collector and the base zero. By definition, the transistor is now at the edge of saturation. Let us call the base current which just saturates the transistor I_{BS} and the dc current gain at the edge of saturation β_F , that is,

$$\beta_{\rm F} = \frac{I_{\rm CS}}{I_{\rm BS}} |_{V_{\rm CB}} = 0$$

where I_{CS} is the collector current at the edge of saturation and is very nearly V_{CC}/R_{C} . Let us now allow the base current to exceed I_{BS} . The collector current remains approximately at its saturation value as further increases in base drive no longer result in a corresponding increase in collector current.

Suppose we suddenly decrease the base current from a value greater than to a value less than $I_{\rm RS}{}^{\bullet}$ We observe a response similar to that

^{*} The proportionality is not strict because the dc current gain β varies slightly with collector current. This relation ($I_C = \beta I_B$) is valid only in the active region.

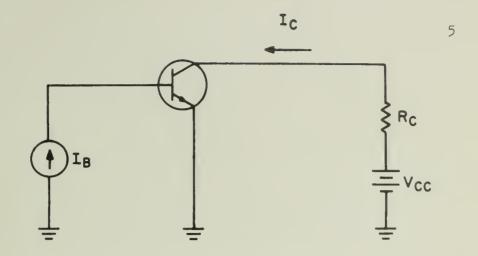


Fig. 1 BASIC TRANSISTOR CIRCUIT

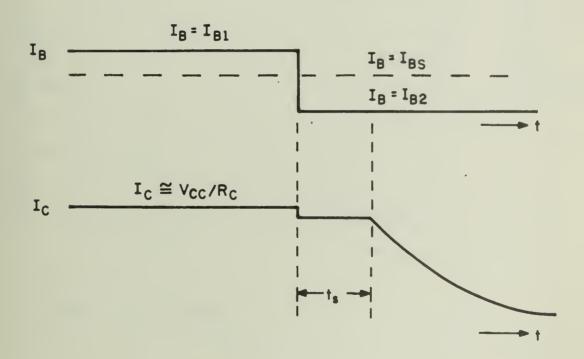


Fig. 2 IDEALIZED INPUT AND OUTPUT WAVEFORMS

shown in Figure 2. Even though the drive is not sufficient to maintain saturation, the collector current remains essentially at its saturation level for a certain amount of time, defined to be the storage time, $t_{\rm S}$. Finally, the collector current decays to its new equilibrium value.

In order to see why a storage time exists, let us consider the minority carrier density in the base region under different conditions of transistor operation. Refer to Figure 3. When the transistor is in the cut-off region, the minority carrier density in the base region is very small (curve C). As we increase the base drive toward I_{pq} , the minority charge carrier density in the base increases toward curve SA. The area under curve SA is denoted by Q_{RS} , the base charge when the transistor is just saturated. As the base drive is increased to an amount $I_{py} > I_{ps}$, the corresponding base charge increases by an amount $Q_{\rm py}$, the "excess saturation charge." It is this excess base charge that must be removed before the transistor can come out of saturation. The storage time $t_{\text{\tiny C}}$ is simply the time necessary to remove the excess saturation charge. It is shown in the next section that the storage time can be predicted with the knowledge of a saturation charge analysis parameter, the dc current gain of the transistor, and the currents supplied to the transistor. The analysis follows that originally developed by Beaufoy and Sparkes.

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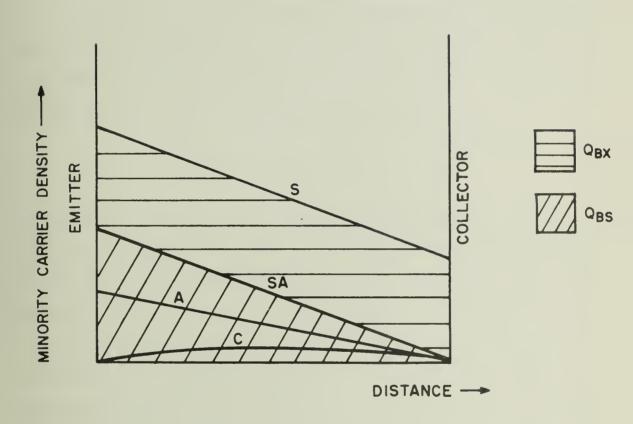


Fig. 3 MINORITY CARRIER DENSITY IN THE BASE REGION

3. THE CHARGE ANALYSIS PREDICTION EQUATION 1-7

Consider the excess minority carrier charge Q_B in the base region of a transistor. The charge Q_B is not the total charge in the base; the total charge in the neutral base region is always zero. Rather, Q_B refers only to the excess of minority charge over the corresponding charge in the steady-state with no current flowing. This charge can be changed by recombination or by the flow of a current into or out of the base region. Let $i_B(t)$ be the current flowing into the base region at any time t. Then conservation of charge (i.e., the continuity equation) requires that

$$i_{B}(t) = \frac{dQ_{B}}{dt}(t) + \frac{Q_{B}}{\tau_{B}}$$
 (1)

where τ_B is the mean lifetime of minority carriers in the base. In the steady-state, with a constant base current $i_B(t) = I_B$, we have $Q_B = \tau_B I_B$. This relationship applies only up to the edge of saturation where the base charge is Q_{BS} and is maintained by a base current I_{BS} . When the transisis in saturation, the base charge consists of the charge Q_{BS} plus some excess saturation charge Q_{BX} . An additional component of base current I_{BX} is required to maintain the excess charge Q_{BX} . This current depends not only on the amount of charge stored but also on the manner in which this charge is distributed. However, we assume a linear relationship; that is, we assume that there is a one-to-one correspondence between the excess saturation charge and the constant current necessary to maintain it. Effectively, we assume the linear charge distribution in the base region that is depicted in Figure 3 (curve S). Hence, this linear charge analysis model applies only if the excess charge in the base changes slowly enough so that the changes can be regarded as a succession of

steady states and the shape of the charge distribution curve remains relatively unchanged. Accordingly, we write that $Q_{\rm BX} = \tau_{\rm S} I_{\rm BX}$, where $\tau_{\rm S}$ (the saturation charge analysis parameter) is nominally a constant depending only on the geometry of the transistor. In practice, for the sample tested, it was found that this parameter varied considerably with circuit bias conditions. This will be discussed later.

So long as the transistor remains in saturation, the voltages across the junctions remain relatively constant, and it is normally assumed that there are no changes in the charges stored in the junction capacitances. In order to take account of any such changes we must write

$$i_{B}(t) = \frac{dQ_{B}(t)}{dt} + \frac{Q_{B}(t)}{\tau_{B}} + \frac{dQ_{VC}(t)}{dt} + \frac{dQ_{VE}(t)}{dt}$$
(2)

where Q_{VC} and Q_{VE} represent the charges on the collector and emitter junction capacitances respectively. (These charges are measured with respect to the equilibrium condition and become zero when the junction applied voltage is zero.) Unfortunately, these junction capacitances are nonlinear functions of the voltages impressed across them. It has been shown that for an ordinary p-n junction the capacitance varies inversely with voltage as $C = K/V^{1/n}$ where n is usually between two and three. However, for the transistor tested it was found that this relation does not hold except for very small junction applied voltages (less than one volt or so), possibly because of the narrowness of the base region and the close proximity of the two junctions. It was also found that for most test conditions the changes in junction capacitance charges is only a small fraction of the excess saturation charge and hence the error made in neglecting or approximating these effects is

relatively small. A discussion of the measurement of the junction capacity and voltage change is found in Appendix I.

An exact analysis of the dynamic behavior of the transistor, taking into account the nonlinear nature of the charge storage in the junction space-charge layers, is very complicated; we shall not pursue it here. The easiest way to take the effect of the change of these charges into account is to replace the saturation charge analysis parameter τ_S by a "total" parameter T_S which, approximately at least, takes this effect into account. The actual measurement of the parameter, as the ratio of charge removed to current, gives T_S rather than τ_S .

Let us return, then, to the derivation of the preduction equation, replacing τ_S by T_S . Recall that, when the transistor is saturated, $Q_B = Q_{BS} + Q_{EX}.$ The transistor is initially keptin saturation with a base drive $I_{B1} > I_{BS}$, and at t = 0 this current is abruptly lowered to a value $I_{B2} < I_{BS}$ as shown previously in Figure 2. During the storage time, then, $i_B(t) = I_{B2}$, $\frac{dQ_{BS}(t)}{dt} = 0$, and

$$I_{B2} = \frac{dQ_{BX}(t)}{dt} + \frac{Q_{BS}}{\tau_{B}} + \frac{Q_{BX}(t)}{T_{S}}$$
(3)

But $Q_{BS} = \tau_{B}^{I}_{BS}$, so

$$\frac{dQ_{BX}(t)}{dt} + \frac{Q_{BX}(t)}{T_{S}} = I_{BS} - I_{BS}$$
 (4)

Integrating, we obtain directly

$$Q_{BX}(t) = k e^{-t/T_S} + T_S (I_{B2} - I_{BS})$$
 (5)

where k is the constant of integration. Next we apply the condition that at t = 0,

$$Q_{BX}(0) = T_S I_{BX}(0) = T_S (I_{B1} - I_{BS})$$

to obtain $k = T_S(I_{Bl} - I_{B2})$. Hence,

$$Q_{BX}(t) = T_{S}(I_{BL} - I_{B2}) e^{-t/T_{S}} + T_{S}(I_{B2} - I_{BS})$$
 (6)

The storage time t_S is the time when $Q_{BX} = 0$. We have then

$$0 = T_{S}(I_{B1} - I_{B2}) e^{-ts/T_{S}} + T_{S}(I_{B2} - I_{BS})$$
 (7)

Hence,

$$t_{S} = T_{S} \ln \left(\frac{I_{B1} - I_{B2}}{I_{BS} - I_{B2}} \right)$$
 (8)

It is convenient to rewrite Equation (8) as follows,

$$t_{S} = T_{S} \ln \left(\frac{I_{B1} - I_{B2}}{I_{CS/\beta_{F}} - I_{B2}} \right)$$
 (9)

since $I_{CS} = \beta_F \ I_{BS}$ at the edge of saturation. This is the desired result: a storage time prediction formula involving two easily measured transistor parameters which accounts (at least approximately) for changes in the charges stored in the junction capacitances.

Since, for the purposes of this paper, the base pull-out current will always have a negative value (current will actually be removed from the base), it is convenient to reverse its reference direction. When we reference the collector and base drive currents into the transistor and the base pull-out current out of the transistor, we arrive at the alternative expression,

$$t_{S} = T_{S} \ln \left(\frac{I_{B1} + I_{B2}}{(I_{CS/\beta_{F}} + I_{B2})} \right)$$
 (10)

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4. MEASUREMENT CIRCUITRY CONSIDERATIONS

Measurement of the Saturation Charge Analysis Parameter

The "total" saturation charge analysis parameter T_S can be measured as the ratio of charge removed (both excess saturation charge and charge removed from junction capacitances) to excess base drive current by using the circuit of Figure 4. This is the technique originally suggested by Beaufoy and Sparkes, 1 and discussed by Searle, 2 Millman and Taub, 3 and others.

Initially, the transistor is in the steady saturation state, defined by the values of the supply voltages. A negative pulse is applied via the R-C network to the base of the transistor. The rise time of the pulse must be much less than the parameter being measured. A Tektronix 109 Pulse Generator with a rise time of less than 0.25 nanosecond was used. Simultaneously, then, a step of base current $\Delta V/R$ and a step of base charge C ΔV are removed from the base. The magnitude of the pulse must be much greater than the base voltage to insure that the proper charge and current are removed. A value of ΔV = -12 volts was used. The resistor R is adjusted so that the transistor just reaches the edge of saturation (V_{CB} = 0). The differential voltage was observed on a Tektronix 567 Oscilloscope. With this setting of the resistance,

$$\frac{\triangle V}{R} = I_{BS}$$
.

By proper adjustment of the capacitor, it is possible to arrange that $C\triangle V = Q_{BX}(+Q_{VC},+Q_{VE})$ so that the excess saturation charge is removed; if there are any changes in the junction-capacitance stored charges, these charges are also removed. Hence, the transistor makes a step

Fig. 4 CIRCUIT TO MEASURE TS

change from saturation to the saturation-active region boundary. Therefore, we have measured the "total" saturation charge analysis parameter; $\mathbf{T}_{\text{C}} = \text{RC}.$

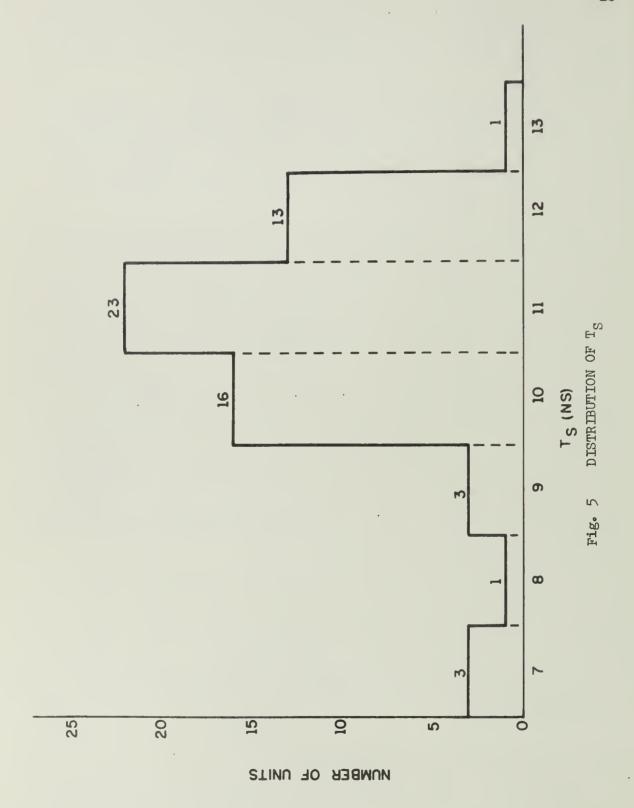
In practice, adjustment is made so that the collector voltage does not change upon application of the pulse, although a slight perturbation occurs just after the pulse is applied. This voltage waveform was also observed on the oscilloscope.

Since accurately calibrated variable capacitors and resistors were not available, both elements were measured at the completion of each measurement. Typical values of resistance and capacity for the transistors tested were 2700 ohms and 4 pf. Such capacitances are relatively difficult to measure with precision; the estimated error in the measurement of this capacity is 0.2 pf or about five percent. There is no difficulty in measuring the resistance accurately. An error of 0.2 pf in the measurement of the capacitance corresponds to an error of about 0.6 ns in T_S . A typical value of T_S is 10 ns at a collector current of 15 mA and a base drive of 15 mA. A histogram indicating the distribution of T_S for the sample is shown in Figure 5.

An alternate test procedure which overcomes the difficulty of repeated measurements of components is suggested by Thornton. ⁴ This method, which uses fixed component values, requires two simultaneous pulses of different amplitudes. The pulse generator used does not produce such pulses.

Measurement of the DC Current Gain Parameter

The dc current gain parameter of interest is the ratio of collector current to base current at the edge of saturation in the common emitter



configuration. Referring to the prediction Equation (10), one can see that β_F is not a particularly critical parameter as long as the base pull-out current does not vanish. For the currents considered, it is easy to show that a unit error in the measurement of β_F would lead to an error of less than 0.04 nanosecond in the predicted value of storage time. (This is shown by evaluating the partial derivative of t_S with respect to β_F for the worst case current conditions.)

The circuit used to measure this parameter is shown in Figure 6. It should be noted that, whereas β_F is defined at the boundary between the active and saturation regions, for convenience it was measured at a nonzero collector-base voltage. The collector-base voltage was never greater than 0.6 millivolt in this test; this is assumed to cause a very negligible error in the storage time prediction.

A Hewlett Packard 3440A Digital Voltmeter was used to monitor voltages across resistors and hence determine the currents. The collector current was determined as the difference between the emitter and base currents.

The mean value of β_F for the sample of transistors is 26.1 at an emitter current of 15 mA. A histogram indicating the distribution of β_F for the sample is shown in Figure 7.

Direct Measurement of Storage Time

The direct measurement of storage can be accomplished by use of the circuit of Figure 8, which is essentially equivalent to the circuit of Ebers and Moll cited by Nanavati. The base drive and collector currents are determined by the settings of the voltage sources, and the base

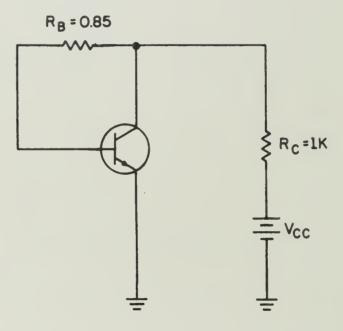
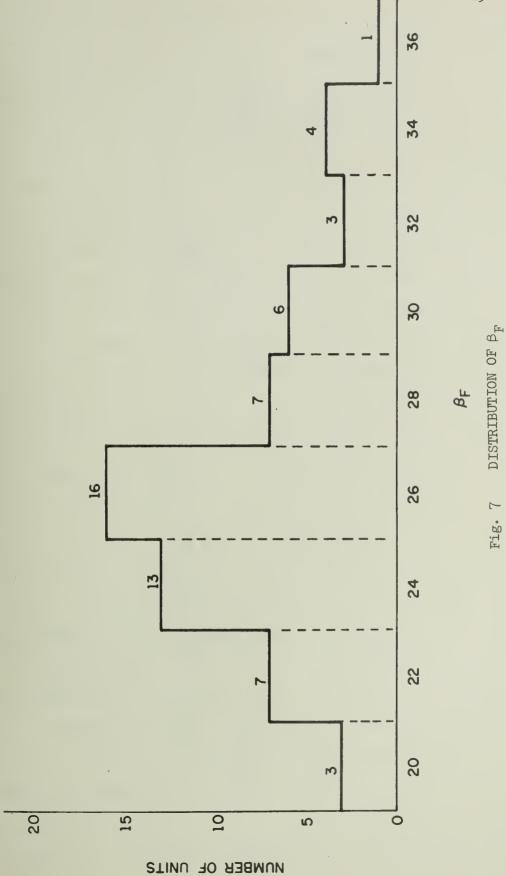


Fig. 6 CIRCUIT TO MEASURE β_F



Fig. 7



pull-out current is determined by the magnitude of the applied pulse. The circuit of Figure 8 differs from the circuit of Ebers and Moll in that the latter requires a pulse generator capable of producing a pulse which is initially offset from zero so that both the base drive and base pull-out currents can be set to desired values by properly adjusting the positive and negative amplitudes of the pulse. The base supply is, of course, not required. It was found that offsetting the Tektronix 109 Pulse Generator deteriorated the pulse rise time considerably (to approximately 3 nanoseconds for the dc offset used). It was decided that this deterioration was not acceptable in the testing of a transistor where typical times measured are on the order of 10 nanoseconds.

In the circuit of Figure 8, the base pull-out current is set by viewing the differential voltage $V_{\rm BB}$,. For a given pulse amplitude, the magnitude of the base pull-out current depends strongly on the base-emitter voltage of the test transistor. The base-emitter voltage varies slightly during the switching process, and as a consequence the base current varies also. Equally important is the unit to unit variation of the base-emitter saturation voltage, which requires an adjustment of the pulse amplitude to yield the desired base current for each transistor, even when the base-emitter voltage remains essentially constant during the switching transient. Since a sample of sixty transistors was to be tested, it was decided that these conditions are not acceptable.

A circuit designed to overcome these difficulties is shown in Figure 9. The circuit contains two constant current generators (regulated by zener diodes). The first current generator supplies a constant base drive current to the test transistor, as long as the pulse is not applied. The magnitude of that current is determined by the variable

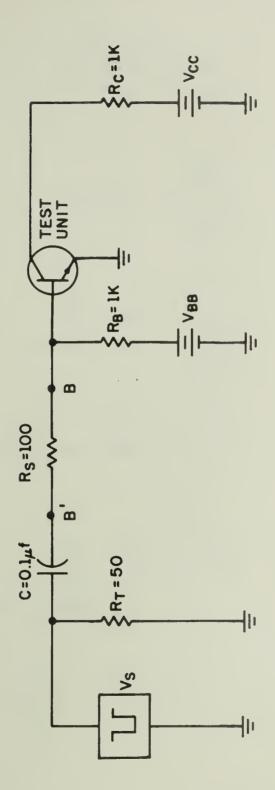
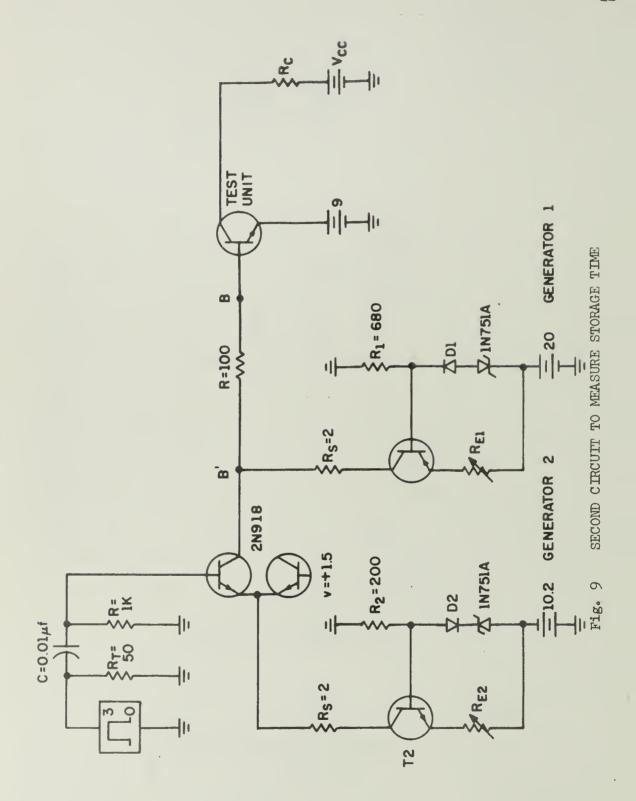


Fig. 8 FIRST CIRCUIT TO MEASURE STORAGE TIME



resistor in the emitter lead. The second current generator conducts a current of approximately $\rm I_{Bl}$ + $\rm I_{B2}$. Again the value of the current is determined by the setting of the emitter resistor. Except when the pulse is applied, this generator draws current through the base-emitter diode of the lower 2N918 transistor. When the pulse is applied, the upper 2N918 supplies current to the generator. The upper 2N918, during application of the pulse, draws current into its collector from both the first current generator and the base of the test transistor. The base drive and pull-out currents are set by viewing the differential voltage $\rm V_{BB}$, on an oscilloscope. The desired saturation collector current is determined by the collector supply voltage. The current switching 2N918 transistors deteriorate the rise time of the current pulse by less than one nanosecond, and the current waveform is not perfectly smooth due, presumably, to the sequential switching of the pair. It was decided that these conditions are acceptable.

It was necessary to offset the emitter of the test transistor to match the dc levels of the rest of the circuit. It would have been preferable to offset the applied pulse to minimize wiring capacity near the test transistor, but, as mentioned previously, an offset produced an unacceptable deterioration of the current pulse rise time.

The storage time was measured with the use of a Tektronic 567

Sampling Oscilloscope with a Type 6Rl Digital Readout Unit, thus facilitating the accumulation of data in a reasonable length of time and eliminating error in reading oscilloscope patterns, except for the initial settings of the base currents.

The current $I_{\rm Bl}$ can be set accurately with no difficulty. Due to the switching of the 2N918 pair and the resulting imperfection in the

base current waveform, the setting of the current I_{B2} is somewhat imprecise. In the worst case the estimated error in the setting of this current is no greater than 0.5 mA. (The lowest value of I_{B2} under consideration is 5 mA.) An error of this magnitude would cause an error in the predicted value of storage time of about one nanosecond, again in the worst case. A typical error would be less than 0.2 nanosecond.

The results of the storage time measurements are presented in the next section.

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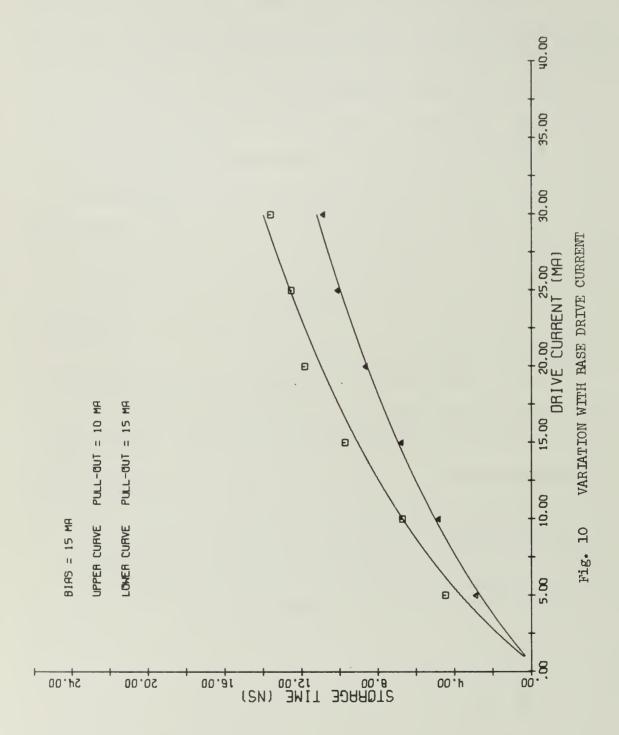
5. DISCUSSION OF EXPERIMENTAL RESULTS

Variation of Storage Time with Base Drive Current and Base Pull-Out Current

In order to test the validity and accuracy of the prediction equation, the storage time was predicted and measured as a function of each of the base currents. In must be pointed out at the outset that the values predicted via Equation (10) employ the measured parameters T_S and β_F , both parameters being measured at the bias conditions of interest and by the methods previously discussed. Hence, any inaccuracy in the determination of these parameters would be reflected as an apparent error in the predicted value of storage time as compared to the direct measurement using the circuit of Figure 9.

It is felt that mean values for the sample carry more statistical significance than measurements for any single unit. All data plotted, quoted, or tabulated refer to mean values for the sample, unless otherwise noted. Data for the first three units, which appear to be representative of the sample, are tabulated in Appendix II. It is seen there that typical deviations of predicted times relative to measured times are about 7 per cent, although the single highest deviation is 23.6 per cent which represents an absolute deviation of 0.7 ns.

The computer-generated plot of mean predicted storage time as a function of base drive current for two different values of base pull-out current is shown in Figure 10. The mean measured data are also plotted on that figure for comparison purposes. The largest absolute deviation of predicted storage time from a measured value is 0.9 ns which occurs on the upper curve ($I_{B2} = 10 \text{ mA}$) of Figure 10 at a drive current of 20 mA. This corresponds to a percentage deviation of about 7 per cent. The



largest percentage deviation (17 per cent) occurs on the upper curve at a drive current of 5 mA. The absolute deviation at that point is 0.8 ns. The mean (unsigned) deviation of the (mean) predicted value relative to the (mean) measured value is slightly less than 5 per cent.

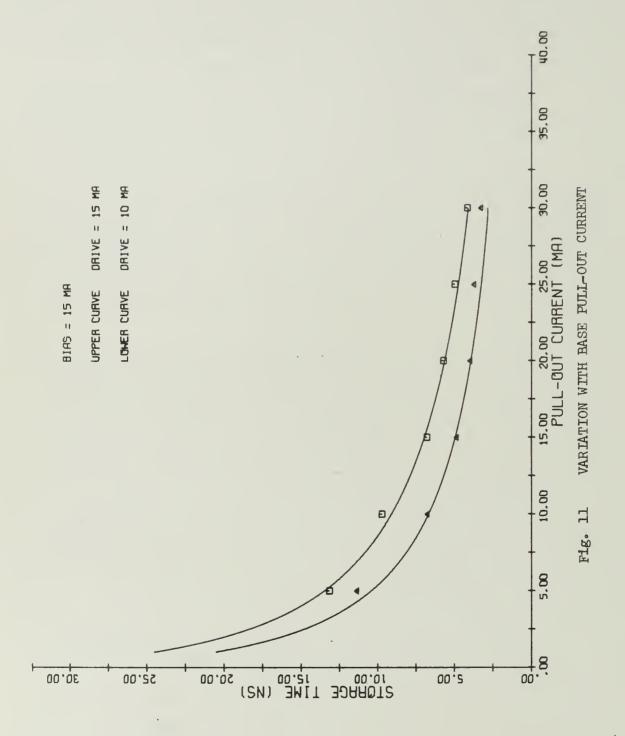
The computer-generated plot of storage time as a function of base pull-out current is shown in Figure 11. The largest absolute deviation here is also 0.9 ns which occurs on the lower curve (I_{Bl} = 10 mA) at a pull-out current of 5 mA. The largest percentage deviation occurs on the lower curve at a pull-out current of 30 mA. The absolute deviation at that point is 0.4 ns or about 13.4 per cent. The mean deviation for the variation with pull-out current is again slightly less than 5 per cent.

The computer programs necessary to generate the plots of Figures 10 and 11 are listed in Appendix III. The IBM 7094 computer was used to generate the data for the predicted curves, and these curves and the measured data points were plotted by the Calcomp Plotter.

Variation of Storage Time with Collector Current and Voltage

As one can readily see from Equation (10), for moderate collector currents (on the same order as the base drive and pull-out currents), the storage time prediction is relatively free of variation with collector current since that current is divided by the current gain of the transistor. The above is true under the assumption that the saturation charge analysis parameter is relatively constant and independent of collector current and voltage. Recall that the collector current we are discussing is the saturation collector current (approximately $V_{\rm CC}/R_{\rm C}$).

As shown in Table 1, it was found that such was not the case for



the transistor tested. Analogous data for the first three units are found in Appendix II.

TABLE 1 $R_{c} = 1000^{S} \text{ohms}$ $(R_C = 500^{\circ} \text{ohms})$ IC mA ns ns 2 18.6 16.9 11.4 5 6.7 6.8 10 5.9 6.8 15 6.4 20 25 30

The storage time was measured at several values of collector current for two different values of load resistance; both base currents were held fixed at 15 mA.

It should be noted that, for collector currents below 10 mA, the storage time varied considerably and in a way that is totally unpredicted by Equation (10) and the theory leading to its development. For collector currents in excess of 10 mA, the storage time is relatively constant. The variation that does exist is still in excess of that predicted and cannot be explained by inaccuracies in measurement or variation of the current gain parameter, although the latter accounts for a small part of the variation.

It should also be noted that the storage time varied somewhat with load resistance, although this variation is fairly small compared to the variation with collector current.

Sparkes also found that the charge analysis parameter varies in an

unpredictable way with collector current, although he also observed a variation of the parameter with base drive current. Mention is also made of this variation in the <u>Switching Transistor Handbook</u>. Such unpredicted variation of storage time with collector current is also illustrated in <u>The Semiconductor Data Book</u>. The data listed in Tables 2 and 3 are read from graphs presented in that book and refer to test conditions which are comparable to those under which the data of Table 1 were obtained in the sense that, to a good approximation, $t_S = 0.69 \, T_S$. In particular, the test condition for the data of Tables 2 and 3 is $I_C = 10 \, I_{Bl} = 10 \, I_{B2}$.

Table 2 refers to a 2N2481 transistor and Table 3 refers to a 2N3250 unit; both transistors are silicon switching units. It is most interesting to note that the data of Table 2 closely parallel those of Table 1, (both curves being convex), whereas the data of Table 3 are read from a curve which is clearly concave.

TAI	BLE 2
I _C	^t s
<u>mA</u>	<u>ns</u>
2 5 10 15 20 25 30	20 12 8.0 6.2 5.9 6.0 6.0

TABLE 3

$^{\mathrm{I}}\mathrm{_{C}}$	${\sf t}_{\sf S}$
<u>mA</u>	ns
2 5 10 15 20 25 30	80 110 125 120 115 105 98

REFERENCES

- J. J. Sparkes, "A Study of the Charge Control Parameters of Transistors," IRE Proceedings, 48:1696-1705, October, 1960.
- 2 <u>Switching Transistor Handbook</u>, pp. 115-128.
- 3 The Semiconductor Data Book, pp. 8-147, 8-210.

6. CONCLUSION

It has been found that the charge analysis prediction Equation (10) employing the "total" saturation charge analysis parameter T_S gives acceptable predictions of the variation of storage time with both base currents provided that both T_S and β_F are measured at the proper collector bias current and voltage. Typical deviations, for the sample tested, were about 5 per cent.

It was also found that the charge analysis parameter T_S and hence the storage time vary considerably with collector current for very low values of collector current (less than 10 mA), but appear to stay relatively constant at higher values of current. The parameter also varies slightly with load resistance.

The $\underline{\text{Transistor}}$ $\underline{\text{Switching}}$ $\underline{\text{Handbook}}^1$ offers a possible explanation of the variation of $\underline{\text{T}}_S$ with bias conditions. A large fraction of the charge injected from the collector could be stored in regions of the base distant from the emitter where surface lifetime could have an appreciable effect. The amount of charge in the area influenced by the surface would be dependent on the bias conditions. Storage of charge in the collector can also considerably modify the effective charge analysis parameter.

As collector current is increased, the drop across the collector resistance $r_{\rm C}$ increases altering the internal biasing to cause more of the collector injection to occur in the region directly under the emitter. More of the active part of the transistor is now in saturation causing storage time to be partly determined by the rate of diffusion of carriers, stored in the collector, back into the base. Thus, $T_{\rm S}$ is not a constant, but is composed of the lifetimes of various regions of the transistor.

Sparkes 2 also indicates the explanation that a significant portion of saturation charge diffuses away from the region of the base which lies between the emitter and collector, thus affecting the lifetime of the stored charge. He also points out that, at low current levels, the change of the collector depletion layer thickness as the transistor is taken from the edge of saturation into saturation should necessitate the injection of extra base charge leading to higher values of $T_{\rm S}$.

It is reasonable to conclude, then, that for the transistor and for the ranges of currents under consideration, Equation (10) provides a suitable prediction equation for storage time if and only if T_S is measured at the proper bias condition or if the collector current is kept above 10 mA. Even in the later case it would be preferable to measure the parameters at the desired bias condition.

In practical switching circuits, it is common that the collector current exceeds 10 mA by a considerable margin, so that the variation in $T_{\rm S}$ would be expected to be small. However, it must also be kept in mind that practical switching circuits do not usually provide constant or exactly known base currents or load resistances, so that, in some situations, application of the prediction equation may yield only a crude approximation to the actual storage time. Further, it must be borne in mind that these conclusions are valid only for the transistor tested and over the range of currents considered, although qualitatively similar results could be expected for other transistors of similar construction. The transistors tested were selected from a sample of 2N3Q11 transistors manufactured in 1964 by Texas Instruments and purchased by the Digital Computer Laboratory under a special specification list. They are planar, passivated, epitaxial silicon units.

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APPENDIX I JUNCTION CAPACITY CONSIDERATIONS

In an effort to experimentally separate the excess saturation charge from the junction capacity stored charge, the junction capacitances were measured as functions of (reverse) voltage. Then, with a knowledge of the excursions of junction applied voltages, the junction capacitances, and the pull-out current, one can determine the portion of storage time which is devoted to removing excess saturation charge and the portion which is devoted to removing junction capacity stored charge.

To this end, the junction capacitances were measured with a Boonton Model D-74 capacitance bridge with a variable internal reverse bias. If the junction areas behave as true capacitors, then the charge stored when a reverse voltage is applied will be the same, in magnitude, as when a forward voltage of the same magnitude is applied. It will be assumed that this is the case.

Combining the storage time measurements of Table 1 with a knowledge of the junction capacitances and voltage excursions, one can then complete Tables 4 and 5 which correspond to load resistances of 1000 ohms and 500 ohms, respectively. In both tables, t_Q represents the amount of time necessary to remove the junction capacity charges.

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TA	DT	1.0	- 71
1.6	$\perp > \perp$	alia -	-+

I _C	ts	^t Q	T_S	τ _S
<u>mA</u>	ns	ns	ns	ns
2 5 10 15 20 25 30	18.6 11.4 6.8 6.8 6.4 6.5	0.9 0.8 0.7 0.6 0.5 0.4	27.2 16.8 10.2 10.4 9.9 10.3 10.9	26.0 15.6 9.2 9.5 9.2 9.7 10.3
		TABLE 5		
I _C	ts	^t Q	TS	τ _S
<u>mA</u>	ns	ns	ns	ns
2 5 10 15 20 25 30	16.9 6.7 5.9 6.2 6.3 6.6 6.6	0.7 0.7 0.7 0.6 0.6 0.5	24.6 9.9 8.9 9.5 9.8 10.4 10.7	23.6 8.8 7.9 8.5 9.0 9.6 9.9

APPENDIX II LISTING OF DATA

Data indicating the variation of storage time with base and collector currents for the first three units are listed in the tables which follow immediately.

For reference and completeness purposes, all measured data are listed on succeeding pages. Relevant test conditions accompany these data. The term $t_{\mbox{WIRING}}$ represents the time allotted to discharging the wiring capacitance (about 1.7 pf); $t_{\mbox{WIRING}}$ must be subtracted from $t_{\mbox{S}}$ to obtain the actual storage time of the transistor.

TABLE 6 $(I_{C} = 15 \text{ mA}, I_{BO} = 10 \text{ mA})$

I _{Bl}	Measur Unit l	ed Storag Unit 2	e Time Unit 3	Predic Unit 1	ted Storag Unit 2	ge Time Unit 3
<u>mA</u>	ns	ns	ns	ns	ns	ns
5 10 15 20 25 30	4.0 6.2 8.4 10.1 11.7 12.7	3.8 5.8 7.7 9.3 9.9	4.9 7.0 10.2 12.9 13.7 15.0	3.6 6.6 8.9 10.8 12.3 13.7	3.3 6.0 8.1 9.9 11.3 12.6	4.1 7.5 10.1 12.3 14.1 15.7

TABLE 7 $(I_{C} = 15 \text{ mA, } I_{B2} = 15 \text{ mA})$

I _{Bl}	Measure Unit l	d Storage Unit 2		Predict Unit 1	ed Storage Unit 2	
<u>mA</u>	ns	ns	ns	ns	ns	ns
5 10 15 20 25 30	2.8 4.8 6.7 7.8 9.2 10.3	2.6 4.5 6.0 6.9 8.1 8.1	3.1 5.3 7.3 9.4 11.1 11.9	2.6 4.9 6.8 8.3 9.7 10.9	2.4 4.5 6.2 7.7 8.9	2.9 5.6 7.7 9.5 11.1 12.5

TABLE 8 $(I_{C} = 15 \text{ mA, } I_{Bl} = 10 \text{ mA})$

I _{B2}	Measure Unit l	ed Storage Unit 2	Unit 3		ed Storag Unit 2	
mA	ns	ns	ns	ns	ns	ns
5 10 15 20 25 30	9.4 6.2 4.8 3.8 3.5 3.0	8.8 5.8 4.5 3.8 3.7 3.1	11.7 7.0 5.3 4.0 3.9 3.4	10.2 6.6 4.9 3.9 3.2 2.8	9.4 6.0 4.5 3.6 3.0 2.5	11.7 7.5 5.6 4.4 3.7 3.2

TABLE 9 $(I_{C} = 15 \text{ mA}, I_{Bl} = 15 \text{ mA})$

I _{B2}	Measure Unit l	d Storage Unit 2	Time Unit 3	Predicted Unit 1		Time Unit 3
<u>mA</u>	ns	ns	ns	ns	ns	ns
5 10 15 20 25 30	12.8 8.4 6.7 5.6 4.6 4.1	10.5 7.7 6.0 5.4 4.7 4.0	14.5 10.2 7.3 6.0 5.2 4.4	13.2 8.9 6.8 5.5 4.6 4.0	12.1 8.1 6.2 5.0 4.2 3.7	15.0 10.1 7.7 6.3 5.3 4.6

TABLE 10

ns

$$(I_{Bl} = 15 \text{ mA}, I_{B2} = 15 \text{ mA}, R_{C} = 1000 \text{ ohms})$$

ns

2	1 7•5	17.4	19.2
5	12.3	9.0	12.3
10	6.4	5.9	7.2
1 5	6.7	6.0	7.3
20	6.0	5.3	6.8
25	5•7	5.2	7.0
30	5•7	5.1	7.3

ns

TABLE 11

(I_{Bl} = 15 mA, I_{B2} = 15 mA, R_{C} = 500 ohms)

Measured Storage Time
I_C Unit 1 Unit 2 Unit 3

<u>mA</u>	ns	ns	ns
2 5 10 15 20 25 30	15.4 6.3 5.8 6.0 5.7 5.7	16.4 6.2 5.7 5.1 4.9 4.9	15.5 6.8 6.2 6.7 6.9 7.0
20	J• 1	マ・フ	1.0

TABLE 12

Unit	β_{F} (I $_{\mathrm{E}}$ = 15 mA)	Unit	$\beta_{\rm F}$ (I _E = 15 mA)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30	26.8 26.8 25.6 24.6 22.3 26.2 26.6 23.2 28.8 20.3 24.1 21.4 22.3 25.7 33.6 31.0 24.6 29.5 29.5 28.1 22.7 26.1 28.1 25.7 24.6 25.7 24.6 25.7 24.6 25.7 24.6 25.7 24.6 25.7 24.6 25.7 24.6 25.7 24.6 25.7 26.1 28.1 25.7 24.6 25.7 24.6 25.7 26.1 28.1 25.7 24.6 25.7 24.6 25.7 24.6 25.7 26.1 28.1 25.7 26.1 28.1 25.7 26.1 28.1 25.7 24.6 25.7 24.6 25.7 26.1 26.1 26.1 27.6 27.7 26.1 28.1 25.7 24.6 25.7 24.6 25.7 24.6 25.7 24.6 25.7 24.6 25.7 26.1 26.1 26.1 27.7 26.1 27.7 27.6 27.7	31 32 33 34 35 36 37 38 39 41 42 43 44 45 47 48 49 50 51 52 53 54 55 56 57 58 59 60	24.1 24.6 24.1 34.5 29.5 26.8 24.1 27.4 24.6 23.7 35.5 28.1 28.8 22.7 32.6 28.1 31.0 23.6 33.5 30.9 26.2 26.2 26.2 26.2 24.1 28.7 26.2 26.2 26.2 26.2 26.2 26.2 26.2 26.2 26.3

TABLE 13 $(I_C = 15 \text{ mA}, I_{B1} = 15 \text{ mA})$

Unit	R K ohms	C <u>pf</u>	T S ns	Unit	R K ohms	C pf	T _S
1 2 3 4 5 6 7 8 9 10 11 2 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30	2.7 2.8 2.8 2.7 2.8 2.8 2.7 2.8 2.8 2.7 2.8 2.8 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.7 2.8 2.7 2.7 2.7 2.7 2.7 2.7 2.7 2.7 2.7 2.7	3.5.2.9.4.2.4.8.8.4.0.8.6.0.0.0.8.0.5.0.4.7.4.2.5.1.1.2.0.5.4.3.3.3.4.3.3.4.4.2.4.2.4.4.3.2.3.4.4.4.4	10.3 9.45 11.8 10.9 9.5 11.3 11.9 10.6 10.3 9.5 11.2 10.6 10.1 11.2 10.8 10.8 7.7 11.2 6.9 10.8 11.9 10.3 6.6 8.65 12.2 11.5 11.7 10.4 11.7	31 33 33 33 33 33 33 33 44 44 45 46 47 48 49 50 50 50 50 50 50 50 50 50 50 50 50 50	2.8 2.8 2.8 2.7 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.8 2.7 2.7 2.8 2.7 2.7 2.7 2.7 2.7 2.7 2.7 2.7 2.7 2.7	3.4.0.0.9.7.4.6.9.1.0.0.9.9.9.2.8.3.5.5.9.5.4.1 3.3.4.4.4.3.3.4.4.4.3.3.4.4.4.4.3.3.3.4.4.4.4.3.3.3.4.4.4.4.3.3.3.4.4.4.4.4.3.3.3.4.4.4.4.4.4.3.3.3.4.4.4.4.4.4.4.3.3.3.4	10.9 10.1 11.2 7.3 10.8 10.0 10.9 11.9 11.2 11.2 9.75 10.0 11.9 10.65 10.8 10.4 10.7 10.1 11.3 12.7 11.6 12.15 12.15 10.7 9.3 9.5 11.1

TABLE 14A

Unit	t _{Sl}	t _{S2}	t _{S3}	t _{S4}	Unit	^t sl	t _{S2}	t _{s3}	t _{S4}
	ns	ns	ns	ns		ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 11 2 13 14 15 16 17 18 19 21 22 32 4 25 6 27 28 29 30	17.73 17.63 19.40 15.64 18.95 20.05 19.20 19.16 18.76 19.80 19.23 17.96 20.05 19.60 19.21 17.07 19.22 16.64 15.69 22.26 18.29 15.75 17.04 21.60 20.29 20.20 19.45 19.17	12.56 9.26 12.58 12.41 8.41 12.30 13.80 12.20 11.63 12.91 12.20 11.46 13.14 12.60 12.02 8.36 12.20 8.21 8.62 13.64 11.60 7.94 8.27 13.78 13.40 12.99 12.85 11.80 12.31	6.65 6.16 7.40 7.43 6.20 7.39 8.18 7.16.44 7.6.60 7.40 7.40 7.5.20 7.5.20 7.5.20 7.5.20 7.7.5.20 7.7.5.20 7.7.5.20 7.7.6.60 7.7.7.60 7.7	6.90 6.22 7.50 7.44 6.35 7.69 8.15 7.22 7.06 6.70 7.13 6.75 7.35 7.29 7.09 5.00 7.32 4.52 7.08 7.91 4.32 5.72 8.12 7.54 6.48 7.70 6.76 7.79	31 32 33 33 33 33 33 33 34 41 41 41 41 41 41 41 41 41 41 41 41 41	19.25 17.86 20.24 17.20 20.02 18.39 19.27 18.94 19.20 17.38 17.60 19.69 19.48 19.29 16.97 19.41 18.83 18.60 19.00 19.78 18.98 19.32 20.03 19.11 17.31 17.80 19.47	12.09 11.39 13.00 8.36 13.30 11.60 12.11 12.14 12.01 10.58 11.56 11.84 13.63 9.59 12.65 12.38 12.23 8.67 12.43 11.59 11.42 12.22 13.56 12.24 13.61 13.40 12.21 8.41 9.83 12.66	7. 27 6. 67 7. 61 5. 96 6. 80 7. 60 7. 60 7. 38 7. 60 7. 98 1. 40 6. 81 7. 44 6. 85 7. 00 7. 76 8. 47 8. 68 7. 68 8. 41 7. 68 8. 47 8. 68 7. 68	7.11 6.66 7.24 4.72 7.88 6.68 7.86 7.86 7.10 7.86 6.53 6.69 7.86 7.10 7.16 6.66 7.55 7.73 8.07 8.02 7.46
Test	:	:	1	2		3	4		
	ohms)	10	000	1000	1	000	1000		
I _C (1	mA)		2	5		10	15		
IBl	(mA)		15	15		15	15		
I _{B2}	(mA)		15	15		15	15		
V _{CB} (SAT) (V	- 2.	. 30	-2.30		.15	-2.17		
V _{CE(}	SAT) (V) 0.0		0.072		076	0.093		
twir	ING (ns) 0.	26	0.26	0	. 24	0.25		

TABLE 14B

Unit	t _{S5}	t _{s6}	t _{S7}	t _{S8}	Unit	t S5	^t s6	t _{S7}	t _{s8}
	ns	ns	ns	ns		ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 30 30 30 30 30 30 30 30 30 30 30 30	6.20 5.58 7.00 6.81 5.71 7.83 6.66 6.48 6.48 6.68	5.90 5.40 7.24 6.71 5.81 11.10 6.12 5.83 7.01 6.34 6.60 6.34 6.60 6.34 6.60 6.56 6.56 7.61 6.70 6.82 7.61 7.82 7.61 7.82 7.61 7.82 7.61 7.82 7.61 7.82 7.61 7.82 7.61	5.93 5.33 7.51 7.03 5.45 8.23 11.44 6.60 6.21 5.70 7.32 6.36 5.78 4.00 6.61 4.38 6.01 10.57 6.18 3.60 4.87 11.25 7.13 8.26 8.26	15.62 16.58 15.71 18.39 17.85 16.71 17.61 17.28 17.15 17.19 17.44 17.02 16.74 17.63 17.45 17.24 16.63 17.01 16.38 16.44 15.67 16.78 17.82 17.73 17.60 17.04 17.14 17.37	31 32 33 33 33 33 33 34 44 44 44 44 45 55 55 55 55 56 56 56 56 56 56 56 56 56	6.74 6.22 6.77 6.22 6.77 6.62 6.61 6.13 6.13 6.13 6.13 6.13 6.13 6.13	6.58 5.98 6.60 4.15 8.60 5.77 6.30 8.16 6.49 6.18 5.71 6.21 6.61 6.60 5.81 6.60 7.50 8.64 9.71 6.60 7.83	7.01 5.74 7.26 4.20 8.74 6.60 6.36 6.20 5.69 5.69 5.60 6.30 7.30 7.30 7.30 7.30 8.41 9.21 7.61 8.65 8.65	17.35 16.55 17.69 16.86 17.58 16.69 17.18 16.48 17.09 18.30 16.60 16.80 17.61 16.43 17.25 17.34 17.28 18.30 17.40 17.51 16.96 16.93 17.15 16.90 16.94 17.65 17.12
Test:			5	6		7	8		
R _C (o		10	00	1000	10	000	500		
I _C (m	A)		20	25		30	2		
I _{Bl} (mA)		15	15		15	15		
I _{B2} (mA)		15	15		15	15		
V _{CB(S}	(V)	-2.		-2.16	-2.		-1.94		
VCE(S	(V)	0.1	09	0.106	0.1	L02	0.057		
tWIRI	NG (ns)	0.	24	0.25	0.	25	0.22		

TABLE 14C

Unit	t _{S9}	t _{SlO}	t _{Sll}	t _{S12}		Unit	t _{s9}	t _{SlO}	tsll	t _{S12}
	ns	ns	ns	ns			ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 24 25 26 27 28 29 30	6.49 6.40 7.00 6.81 6.34 7.00 8.59 6.69 6.61 7.01 6.55 7.08 6.68 6.73 6.18 6.41 7.78 6.61 7.12 7.12 7.12 7.16	6.04 5.60 6.40 6.25 5.80 6.80 6.25 6.80 6.20	6.18 5.34 6.61 7.41 10.45 6.30 6.41 6.36 6.36 6.36 6.36 6.37 8.37	5.95 5.15 7.07 6.77 5.40 7.51 10.87 6.28 6.28 6.38 6.38 6.38 6.38 6.39 6.17 6.49 6.77 7.88 6.79 6.77 7.88 6.79		31233456678901234567890 323345678901234567890	6.80 6.59 7.05 6.24 7.25 6.60 6.81 7.80 6.61 6.61 7.85 6.81 6.85 6.85 6.85 6.85 6.85 6.85 6.85 6.85	6.20 5.81 6.19 3.50 7.10 5.80 6.04 7.25 6.08 5.78 5.88 6.43 5.79 6.00 6.11 6.20 5.89 6.11 6.20 7.60 1.19 6.92 7.61 5.61 5.61 6.31	6. 41 5. 84 6. 89 7. 79 6. 40 7. 76 6. 40 7. 89 7. 80 7. 80	6.53 5.71 6.31 3.70 8.15 5.70 6.30 7.30 7.30 7.30 7.30 7.70 6.25 6.25 6.25 6.25 6.25 6.25 6.35 7.70 6.35 6.35 7.70 6.35 7.70
Test:	:	9	9	10		11		12		
R _C (o		50		500		500	E.	500		
I _C (m	ıA)		5	10		15		20		
I _{Bl} (mA)	1	-5	15		15		15		
I _{B2} (mA)	1		15		15		15		
V _{CB(S}	(V)	-1.9	93	-1.93		-1.95				
VCE(S	(V) (TAS	0.07	0	0.087	(0.087	0.0	98		
tWIRI	NG (ns)	0.2	2	0.22		0.22	0.	22		

TABLE 14D

Unit	ts13	t _{S14}	ts15	^t s16	Unit	t _{S13}	^t s14	t _{S15}	^t s16
	ns	ns	ns	ns		ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 11 2 13 14 15 16 17 18 19 20 21 22 24 27 28 29 30 30 30 30 30 30 30 30 30 30 30 30 30	5.96 5.14 7.19 6.76 5.72 6.20 6.21	5.89 5.11 7.23 6.71 5.20 7.88 11.52 6.33 6.19 5.70 6.99 6.52 3.78 6.52 3.88 5.99 10.73 6.10 3.33 4.50 11.02 7.11 6.93 7.93 5.88 8.09	4. 15 3. 96 3. 98 4. 96 3. 77 4. 50 4. 50 4. 50 4. 50 4. 50 4. 50 4. 50 4. 50 4. 50 4. 50 5. 60 60 60 60 60 60 60 60 60 60	6.54 6.12 7.01 7.68 7.68 7.68 6.40 7.66 6.84 7.95 6.84 7.95 6.87 7.95 6.87 7.95 6.87 7.95 6.87 7.95 6.87 7.95 6.87 7.95 7.95 7.95 7.95 7.95 7.95 7.95 7.9	31 33 33 33 33 33 33 33 33 44 44 45 47 49 50 51 51 51 51 51 51 51 51 51 51 51 51 51	6.61 5.64 3.61 5.63 8.65 6.38 7.50 6.65 8.00 5.80 5.80 5.80 6.80 7.91 6.80 7.91 6.80 7.91 6.80 7.91 7.91 7.91 7.91 7.91 7.91 7.91 7.91	6.75 7.01 3.65 6.46 6.57 9.52 9.52 9.15 9.15 9.15 9.15 9.15 9.15 9.15 9.15	4.1168 5.559 4.740 5.559 4.740 5.128 8.392 7.098 7.128 8.392 7.098 7.129 8.312 8.559	7.16.41 6.86.34.24.45.66.45.45.45.45.45.45.45.45.45.45.45.45.45.
Test	a •	13	3	14	1 5		16		
R _C (o		50	0	500	1000		1000		
I _C (m		2		30	. 15		15		
I _{Bl} (1		1 5	5		10		
I _{B2} (mA)	1		15	10		10		
V _{CB(S}	(V)	-l <u>.</u> 9	5	-1.94	-1.13		-1.75		
VCECS	(V) (V)	0.10	3	0.150	0.120		0.102		
t _{WIRI}	NG (ns)	0.2	2	0.22	0.19		0.30		

TABLE 14E

Unit	t _{S17}	t _{S18}	t _{Sl9}	t _{S20}	Unit	t _{Sl7}	t _{S18}	t _{S19}	t _{S20}
	ns	ns	ns	ns		ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 1 12 13 4 15 6 17 18 19 20 1 22 24 25 6 27 28 29 30	8.80 8.07 10.53 10.61 8.26 12.41 15.48 9.90 8.99 8.58 11.42 9.37 8.61 9.93 9.86 9.31 7.31 10.02 7.27 8.98 13.61 9.00 7.16 7.88 14.19 11.37 10.56 12.52 8.56 13.11	10.57 9.78 13.42 12.68 9.96 14.20 16.69 12.34 10.65 13.41 11.71 10.38 12.21 11.71 10.83 8.81 11.66 8.60 12.09 15.60 11.95 8.61 9.44 17.54 14.38 13.72 15.40 10.20 15.81	12.34 10.51 14.32 14.04 10.67 15.45 19.39 14.10 12.42 11.61 14.83 13.76 12.11 13.92 13.39 12.78 8.66 13.60 8.30 13.10 16.49 12.82 9.03 17.64 16.01 14.10 15.88 10.83 16.26	13.41 11.63 15.71 15.22 12.35 16.60 21.13 15.52 13.51 12.82 16.27 15.08 13.31 15.27 14.19 13.63 8.86 14.69 8.54 14.10 17.75 13.81 8.58 9.60 19.55 16.39 15.38 17.12 12.32 17.58	31 32 33 33 34 35 36 37 38 39 41 42 34 44 44 45 46 47 48 49 59 59 59 59 59 59 59 59 59 59 59 59 59	9.82 8.56 9.27 7.34 13.11 8.43 9.15 13.15 9.50 9.27 8.34 8.66 12.78 9.34 9.25 8.96 9.34 9.25 8.80 12.15 14.01 14.06 8.42 8.42 8.28 11.13	12.61 10.26 11.08 9.02 15.81 10.26 11.80 16.12 12.46 10.20 10.47 15.46 10.23 11.25 11.39 11.44 12.23 12.41 10.22 11.10 14.81 19.41 17.50 17.34 12.27 10.01 9.85 13.42	12.97 11.22 12.66 8.47 16.21 11.42 12.51 16.66 12.71 13.40 10.90 11.68 15.85 11.09 12.50 12.36 12.42 12.71 12.83 10.92 12.20 15.18 19.79 15.75 17.61 17.47 12.51 10.01 9.49 13.50	13.80 11.68 13.60 8.86 17.47 12.88 13.61 17.99 13.72 14.50 12.54 12.89 17.18 13.66 13.70 13.41 13.39 13.69 13.72 12.43 13.38 16.57 22.32 17.01 19.57 19.15 13.56 12.01 11.17 14.21
Test:		1	.7	18		19	20		
R _C (o		10	00	1000	10	00	1000		
I _C (m			15	15		15	15		
I _{Bl} (15	20		25	30		
I _{B2} (mA)		10	10		10	10		
V _{CB(S}	(V) (TA	-2.	25	-3.02	-3.	55	-4.10		
V _{CE(S}	(V)	0.1	00	0.089	0.0	89	0.086		
t _{WIRI}	/ \	0.	38	0.51	0.	60	0.70		

TABLE 14F

Unit	t _{S21}	ts22	t _{S23}	t _{S24}	Unit	ts21	t _{S22}	ts23	t _{S24}
	ns	ns	ns	ns		ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 11 2 13 4 15 16 17 18 19 20 21 22 23 24 25 6 27 28 29 30	10.72 8.61 12.38 12.01 9.44 12.93 15.80 12.19 10.81 10.01 12.58 11.91 10.56 11.98 12.47 11.12 7.98 11.67 7.77 11.66 13.40 11.10 7.83 8.44 14.82 12.62 12.00 13.21 9.36 13.48	9.58 8.49 11.48 10.83 8.67 11.51 13.86 10.48 10.10 11.18 10.60 10.04 10.11 10.13 10.34 8.30 10.36 7.46 10.57 11.83 11.01 7.56 8.01 12.36 11.31 11.29 11.53 10.13	8.13 7.24 9.72 9.24 7.38 9.77 11.78 8.90 8.79 8.60 9.52 9.06 7.87 8.81 7.18 8.77 8.81 7.18 8.79 6.37 8.98 10.09 10.15 6.46 6.82 10.58 9.64 9.58 9.66	5. 34 5. 54 5. 54 5. 72 5. 33 5. 33 5. 33 5. 33 5. 33 5. 33 5. 34 5. 32 5. 34 5. 32 5. 34 5. 32 5.	31 32 33 34 56 37 38 39 41 42 34 44 45 46 47 48 49 50 51 51 52 52 53 54 56 57 58 59 59 59 59 59 59 59 59 59 59 59 59 59	11.39 9.94 10.76 8.04 13.62 10.03 11.01 14.11 10.98 11.61 9.71 10.20 13.12 9.80 10.69 10.59 11.21 11.14 9.75 11.01 12.80 16.16 13.22 14.89 14.78 10.97 9.26 8.79 11.62	11.01 9.77 9.79 7.80 11.84 9.66 10.68 11.70 10.52 11.00 9.43 9.96 12.02 9.66 10.48 10.52 10.34 11.00 10.91 9.58 10.66 11.57 12.16 12.32 12.16 10.94 8.74 8.36 11.26	9.37 8.41 8.43 6.77 10.10 8.36 9.96 8.99 9.36 8.55 10.24 8.92 9.03 8.83 9.44 8.91 9.84 10.52 10.52 7.26 7.13 9.64	5.58 4.58 5.58 5.69 5.10 6.21
Test:		2.	1	22		23	24		
R _C (o		10	00	1000	10	00	1000		
I_{C} (m			15	15		15	15		
I _{Bl} (mA)		30	25		20	10		
I _{B2} (mA)		15	15		15	15		
V _{CB(S}	(V)	-4.	10	-3.04	-2.	71	-2.03		
VCE(S	(V) (TA	0.0	90	0.094	0.1	.09	0.116		
twiri	NG (ns)	0.	47	0.35	0.	31	0.23		

TABLE 14G

Unit	t _{S25}	ts26	t s27	t _{s28}	Unit	ts25	t _{s26}	t _{S27}	t _{s28}
	ns	ns	ns	ns		ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 24 27 28 29 30 30 30 30 30 30 30 30 30 30 30 30 30	2.92 2.76 3.23 3.10 2.88 3.07 3.04 2.92 3.16 3.05 2.91 3.02 3.10 3.91 3.07 3.10 3.91 3.07 3.10 3.11 3.07 3.10	3.94 3.92 4.19 4.11 3.89 4.12 3.96 4.12 3.96 4.08 4.02 4.22 4.21 4.12 3.75 4.12 3.75 4.14 4.21	3.63 3.70 3.86 3.86 3.86 3.89 3.89 3.89 3.89 3.89 3.89 3.89 3.89	3.13 3.20 3.48 3.36 3.19 3.42 3.32 3.46 3.44 3.42 3.31 3.42 3.39 3.45 3.11 3.42 3.39 3.30 3.45 3.11 3.29 3.36 3.31 3.30 3.31 3.30 3.31 3.31 3.32 3.30 3.31 3.31 3.32 3.32 3.32 3.32 3.32 3.32	31 33 33 33 33 33 33 33 33 34 44 44 45 45 55 55 55 55 55 56 78 90 60 60 60 60 60 60 60 60 60 60 60 60 60	3.06 2.63 2.65 1.79 3.32 2.88 3.03 3.07 3.05 2.66 2.72 3.19 2.91 3.08 2.96 2.97 3.20 3.56 3.32 3.57 3.56 3.57 3.58 3.68 3.69	4.18 4.00 4.25 3.80 4.40 4.20 4.18 4.00 4.21 4.00 4.21 4.00 4.20	3.89 3.67 3.92 3.59 4.03 3.65 3.83 3.76 3.83 3.76 3.99 3.99 3.99 3.99 3.99 3.99 3.99 3.9	3.38 3.17 3.45 3.11 3.53 3.06 3.42 3.32 3.24 3.28 3.44 3.32 3.44 3.36 3.44 3.36 3.44 3.57 3.47 3.57
Test	:	4	25	26	2	27	28		
R _C (o		10	000	1000	10	00	1000		
I _C (m			15	15		15	15		
I _{Bl} (mA)		5	10		10	10		
I _{B2} (15	20		25	30		
V _{CB} (S	(V)	-1.		-1.95	-1.	96	-1.98		
VCE(S	(V)	0.1		0.112	0.1	12	0.115		
tWIRI	(ns)	0.	12	0.17	0.	13	0.11		

TABLE 14H

Unit	t _{S29}	ts30	ts31	ts32	Unit	t _{S29}	t _{s30}	t _{S31}	t _{S32}
	ns	ns	ns	ns		ns	ns	ns	ns
1 2 3 4 5 6 7 8 9 10 12 13 4 15 6 17 8 9 20 1 22 32 4 25 6 27 8 29 30	10.12 9.46 12.39 12.56 9.67 13.62 16.18 11.92 10.13 9.78 13.31 11.56 10.52 12.01 11.45 10.86 8.72 11.57 8.70 11.89 14.32 14.32 14.32 14.32 15.06 9.31 16.15 14.32 15.06 9.92 15.50	13.51 11.16 15.12 14.51 11.16 16.12 19.66 15.10 13.66 12.22 16.77 14.60 12.92 15.04 13.78 13.21 9.31 14.36 7.92 13.58 17.81 13.18 8.29 9.19 18.92 16.71 14.68 16.22 12.31 16.16	5.73 5.66 5.19 6.10 5.00 5.75 6.89 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 6.99 7.53 7.54 7.54 7.54 7.54 7.54 7.54 7.54 7.54	4.70 4.85 5.29 5.15 5.10 5.10 5.10 5.11 5.21 4.97 5.28 5.11 5.28 5.17 5.30 5.31 6.77 5.31 6.77	33333333344445678901234567890 32345678901234567890	12.11 10.12 10.78 8.84 15.46 10.08 11.59 15.32 12.56 12.76 9.80 10.18 15.18 9.95 10.86 10.98 10.96 10.92 12.52 10.36 10.81 14.62 18.42 15.56 17.06 17.18 11.97 9.73 9.37 13.02	13.31 10.98 13.51 9.32 13.48 12.36 13.20 17.52 13.33 13.92 11.98 12.59 16.77 11.98 13.22 12.88 13.24 13.26 11.69 12.92 16.13 20.75 16.48 19.06 18.88 13.02 11.42 10.44 13.78	5·3512004 5·3512004 6·361896 6·3619907 6·3619907 6·3619907 6·3619909 6·361909 6·3619909 6·3619909 6·3619909 6·361909	5. 4. 91 14. 31 15. 4. 5. 91 14. 5. 91 14. 5. 91 15. 14. 5. 91 16. 14. 5. 91 16. 14. 14. 14. 14. 14. 14. 14. 14. 14. 14
Test:	:	2	29	30	3	31	32		
R _C (o		10	00	1000	10	00	1000		
I _C (m			15	15		15	15		
I _{Bl} (10	15		15	15		
I _{B2} (5	5		20	25		
V _{CB(S}	(V)	-2.		-1.98		96	-1.96		
VCE(S	(V)	0.1		0.097		95	0.096		
tWIRI	NG (ns)	0.	70	0.67	0.	17	0.13		

TABLE 14I

Unit	t _{s33}	Unit	t _{s33}
	ns		ns
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30	4.13 4.47 4.36 4.39 4.30 4.33 4.33 4.33 4.33 4.33 4.33 4.39 4.30 4.31 4.31 4.32 4.32 4.62 4.62 4.12 4.43 4.12 4.43 4.33 4.34 4.35 4.36 4.37 4.38 4.38 4.38 4.38 4.38 4.38 4.39	32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 44	4.36 4.48
Test:	33		
R _C (ohms) I _C (mA) I _{Bl} (mA) I _{B2} (mA) VCB(SAT) (V) VCE(SAT) (V) t _{WIRING} (ns)	1000 15 15 30 -1.96 0.096 0.110		

PROGRAM I

```
CALL CPB1
C
      VARIATION WITH BASE DRIVE CURRENT
     ODIMENSION TX(2), TY(2), TAU(60), BETA(60), TIML(1200),
           DRIV1(1200), TIM2(1200), DRIV2(1200), DRIVM1(6),
           TIMM1(6), DRIVM2(6), TIMM2(6), T(60), F(60)
C
     READ MEASURED DATA
      RIT 7,5, (DRIVM1(J), J=1, 6)
  5
      FORMAT (6F10.0)
      RIT 7, 5, (DRIVM2(L), L=1, 6)
      RIT 7,5, (TIMML(M), M=1,6)
      RIT 7, 5, (TIMM2(N), N=1, 6)
      READ TAU AND BETA
C
      DO 10 I = 1,60
      RIT 7, 1, TAU(I), BETA(I)
     FORMAT (2F10.0)
  1
  10 CONTINUE
      BIAS = 15.0
      PULL = 10.0
C
      CALCULATE POINTS FOR FIRST CURVE
      DO 20 K = 1,1161
      XK = K - 1
      DRIV1(K) = 1.0 + XK/40.0
      DO 13 N = 1,60
      F(N) = (DRIV1(K) + PULL)/(PULL + BIAS/BETA(N))
  13 T(N) = TAU(N) * ELOG(F(N))
      XT = 0.0
      DO 14 N = 1,60
  14 \quad XT = XT + T(N)
  20 \text{ TIML}(K) = XT/60.0
      PULL = 15.0
C
      CALCULATE POINTS FOR SECOND CURVE
      DO 30 K = 1,1161
      XK = K - 1
      DRIV2(K) = 1.0 + XK/40.0
      DO 15 N = 1,60
      F(N) = (DRIV2(K) + PULL)/(PULL + BIAS/BETA(N))
      T(N) = TAU(N) * ELOG(F(N))
  15
      XT = 0.0
      DO 16 N = 1,60
  16 \quad XT = XT + T(N)
  30 \text{ TIM2}(K) = XT/60.0
```

```
C
      PLOT AXES AND FIND SCALE FACTOR
      DIMENSION FIELD (2321)
      DO 100 K = 1,1160
      FIELD(K) = TIMl(K)
      DO 200 J = 1,1160
      FIELD(J + 1160) = TIM2(J)
 200
      FIELD(2321) = 0.0
      CALL CCP4SC (FIELD, 6.5, 2321, 1, TY)
      CALL CCP4SC (DRIV1, 8.0, 1160, 1, TX)
      CALL CCP1PL (0.5, 0.5, -3)
     OCALL CCP5AX (0.0,0.0,18HDRIVE CURRENT (MA),-18,
           8.0, 0.0, TX)
     OCALL CCP5AX (0.0,0.0,17HSTORAGE TIME (NS),17,
           6.5,90.0,TY)
      PLOT CURVES
C
      CALL CCP6LN (DRIVI, TIMI, 1160, 1, TX, TY)
      CALL CCP6LN (DRIV2, TIM2, 1160, 1, TX, TY)
C
      PLOT TITLE
      CALL CCP2SY (1.0, 6.0, 0.10, 12HBIAS = 15 MA, 0.0, 12)
     OCALL CCP2SY (1.0, 5.625, 0.10, 30HUPPER CURVE
                                                       PULL-
           OUT = 10 MA, 0.0, 30)
     OCALL CCP2SY (1.0,5.250,0.10,30HLOWER CURVE
                                                      PULL-
         OUT = 15 MA, 0.0, 30)
C
      PLOT MEASURED DATA POINTS
      DO 40 \text{ K} = 1,6
      X = (DRIVML(K) - TX(1))/TX(2)
      Y = (TIMM1(K) - TY(1))/TY(2)
     CALL CCP2SY (X, Y, 0.08, 0, 0.0, -1)
      DO 50 L = 1.6
      X = (DRIVM2(L) - TX(1))/TX(2)
      Y = (TIMM2(L) - TY(1))/TY(2)
  50 CALL CCP2SY (X, Y, 0.08, 2, 0.0, -1)
      CALL CCP1PL (10.0,0.0,-3)
      END OF PLOTTING ROUTINES
C
      CALL SYSERR
```

END

PROGRAM II

```
CALL CPB1
      VARIATION WITH BASE PULL-OUT CURRENT
C
     ODIMENSION TX(2), TY(2), TAU(60), BETA(60), TIML(1200),
           PULL1(1200), TIM2(1200), PULL2(1200), PULLM1(6),
     2
           TIMM1(6), PULLM2(6), TIMM2(6), T(60), F(60)
      READ MEASURED DATA
C
      RIT 7,5, (PULLM1(J), J=1,6)
     FORMAT (6F10.0)
      RIT 7,5, (PULLM2(L), L=1,6)
      RIT 7,5, (TIMML(N), N=1,6)
      RIT 7,5, (TIMM2(M), M=1,6)
      READ TAU AND BETA
C
      DO 10 I = 1,60
      RIT 7,1,TAU(I),BETA(I)
     FORMAT (2F10.0)
  10 CONTINUE
      BIAS = 15.0
      DRIVE = 10.0
      CALCULATE POINTS FOR FIRST CURVE
C
      DO 20 K = 1,1161
      XK = K - 1
      PULL1(K) = 1.0 + XK/40.0
      DO 13 N = 1,60
      F(N) = (PULL1(K) + DRIVE)/(PULL1(K) + BIAS/BETA(N))
  13 T(N) = TAU(N) * ELOG(F(N))
      XT = 0.0
      DO 14 N = 1,60
  14 	 XT = XT + T(N)
  20 \text{ TIML}(K) = XT/60.0
      DRIVE = 10.0
      CALCULATE POINTS FOR SECOND CURVE
      DO 30 K = 1,1161
      XK = K - 1
      PULL2(K) = 1.0 + XK/40.0
      DO 15 N = 1,60
      F(N) = (PULL2(K) + DRIVE)/(PULL2(K) + BIAS/BETA(N))
     T(N) = TAU(N) * ELOG(F(N))
      XT = 0.0
      DO 16 N = 1,60
  16 \quad XT = XT + T(N)
  30 \text{ TIM2}(K) = XT/60.0
      PLOT AXES AND FIND SCALE FACTOR
      DIMENSION FIELD (2321)
      DO 100 \text{ K} = 1,1160
100 \text{ FIELD(K)} = \text{TIML(K)}
```

```
DO 200 J = 1,1160
     FIELD(J + 1160) = TIM2(J)
 200
      FIELD (2321) = 0.0
      CALL CCP4SC (FIELD, 6.5, 2321, 1, TY)
      CALL CCP4SC (PULL1, 8.0, 1160, 1, TX)
      CALL CCP1PL (0.5,0.5,-3)
     OCALL CCP5AX (0.0,0.0,21HPULL-OUT CURRENT (MA),
            -21, 8.0, 0.0, TX)
     OCALL CCP5AX (0.0,0.0,17HSTORAGE TIME (NS),17,
            6.5,90.0,TY)
      PLOT CURVES
C
      CALL CCP6LN (PULLL, TIM1, 1160, 1, TX, TY)
      CALL CCP6LN (PULL2, TIM2, 1160, 1, TX, TY)
      PLOT TITLE
C
      CALL CCP2SY (4.0, 6.0, 0.10, 12 \text{HBIAS} = 15 \text{ MA}, 0.0, 12)
     OCALL CCP2SY (4.0, 5.625, 0.10, 27 HUPPER CURVE
          = 15 MA, 0.0, 27)
     OCALL CCP2SY (4.0,5.250,0.10,27HLOWER CURVE
                                                       DRIVE
           = 10 MA, 0.0, 27)
C
      PLOT MEASURED DATA POINTS
      DO 40 \text{ K} = 1,6
      X = (PULLMl(K) - TX(1))/TX(2)
      Y = (TIMML(K) - TY(1))/TY(2)
  40 CALL CCP2SY (X,Y,0.08,0,0.0,-1)
      DO 50 L = 1,6
      X = (PULLM2(L) - TX(1))/TX(2)
      Y = (TIMM2(L) - TY (1))/TY(2)
      CALL CCP2SY (X, Y, 0.08, 2, 0.0, -1)
  50
      CALL CCP1PL (10.0,0.0,-3)
      END OF PLOTTING ROUTINES
C
      CALL SYSERR
      END
```







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